A Major Threat to Satellites Radio Systems in Low Earth Orbit

Reinaldo Perez
Jet Propulsion Laboratory
8003 South Corona Way, Littleton, CO 80122
phone:303-977-5845, fax:303-9714306, email:ray.j.perez@lmco.com

Introduction

Over the last two years several satellites in Low Earth Orbit (LEO) and geosynchronous orbit (GEO) have experienced serious or catastrophic failures including interruption of desired communications due to especially to non linear interference. It has been shown that severe electrostatic discharges from spacecraft dielectric surfaces can sustain high discharge currents capable of disabling key avionics components posing a threat to satellite communications.

Short Summary

Surface charging of spacecraft surfaces in LEO and GEO orbit environments is caused primarily by electrons with high energies during magnetospheric substorms. The potentials reached during charging events depends on the total current balance among several types of effects. Differential charging occurs when parts of a spacecraft are charged at different negative potentials relative to each other. In this type of charging strong electric fields develop. When the electric fields exceed critical values electrostatic discharges (ESD) can cause not only EMI but can pose potential threats to spacecraft hardware.

The physics involved in the charging mechanisms in spacecraft at geosynchronous and low earth orbits is addressed. We address the discharge mechanism involved in an ESD event. Modeling the discharge mechanism from solar array surfaces and thermal blankets surfaces as shown in Figure 1. The induced current from these ESD events can cause severe satellite malfunction in communication systems.

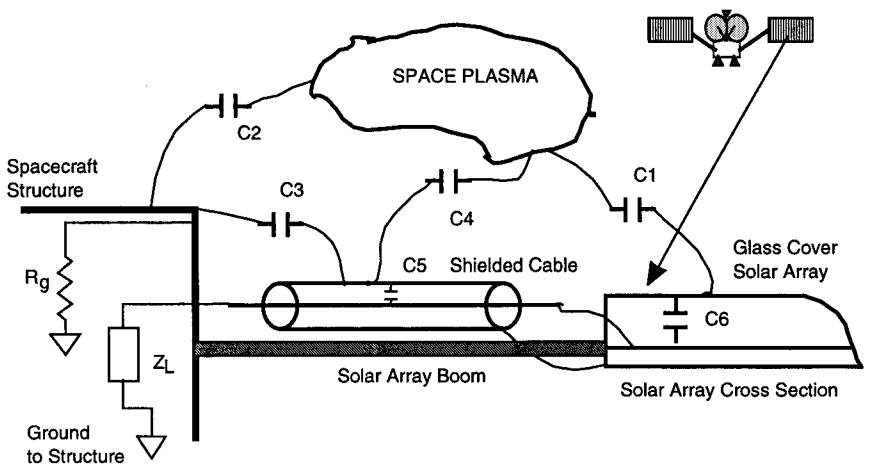

Figure 1. Lumped Element Parameters for ESD Event Between a Solar Array and Cable.

References:

[1] Launchspace Magazine," Major Space Losses 1994-1998," October 1998.

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Reinaldo Perez
Jet Propulsion Laboratory
California Institute of Technology
Pasadena, CA

OUTLINE

1) The ESD threat to satellite radio systems

2) Description of the threat. Charging and ESD in space

3) ESD effects on spacecraft electronics

4) ESD effects on radio systems

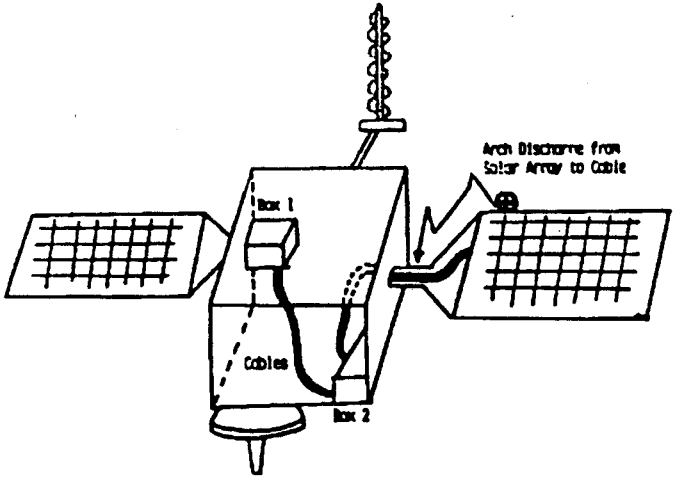
5) Modeling and analysis of ESD events

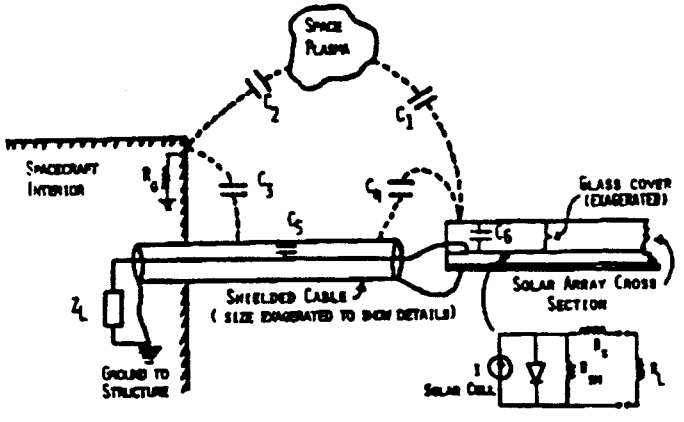
6) Conclusion

The ESD Threat to Satellite Radio Systems

ESD Effects on Satellites

Simply stated: Electroststic discharge events in satellites can disable a satellite.





Description of the Threat. Charging and ESD in Space

Space Environment and Interference

9.0 Introduction.

The region of space dominated by the plasma surrounding the earth is called the magnetosphere. A popular visualization of the magnetosphere is shown in Figure 9.1.

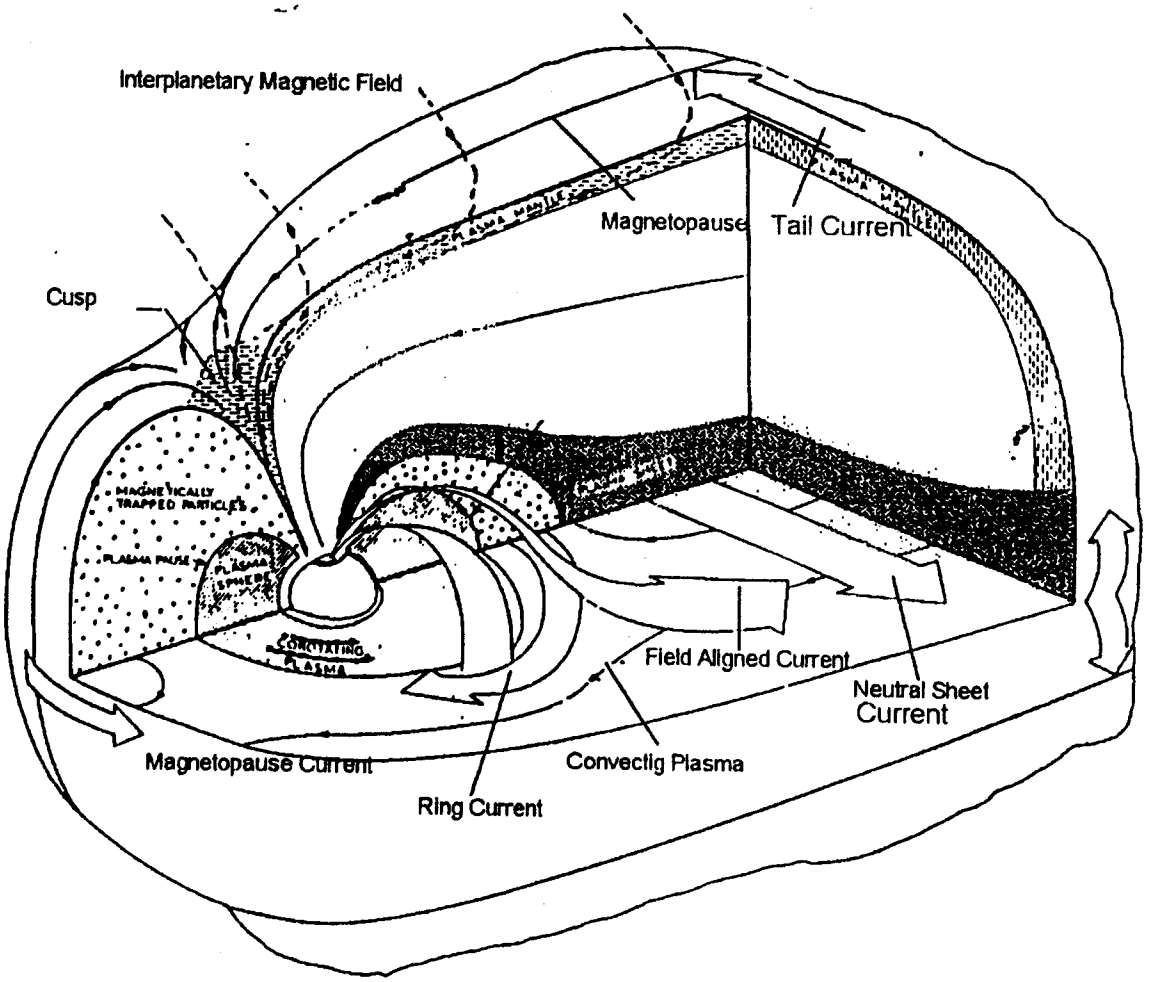
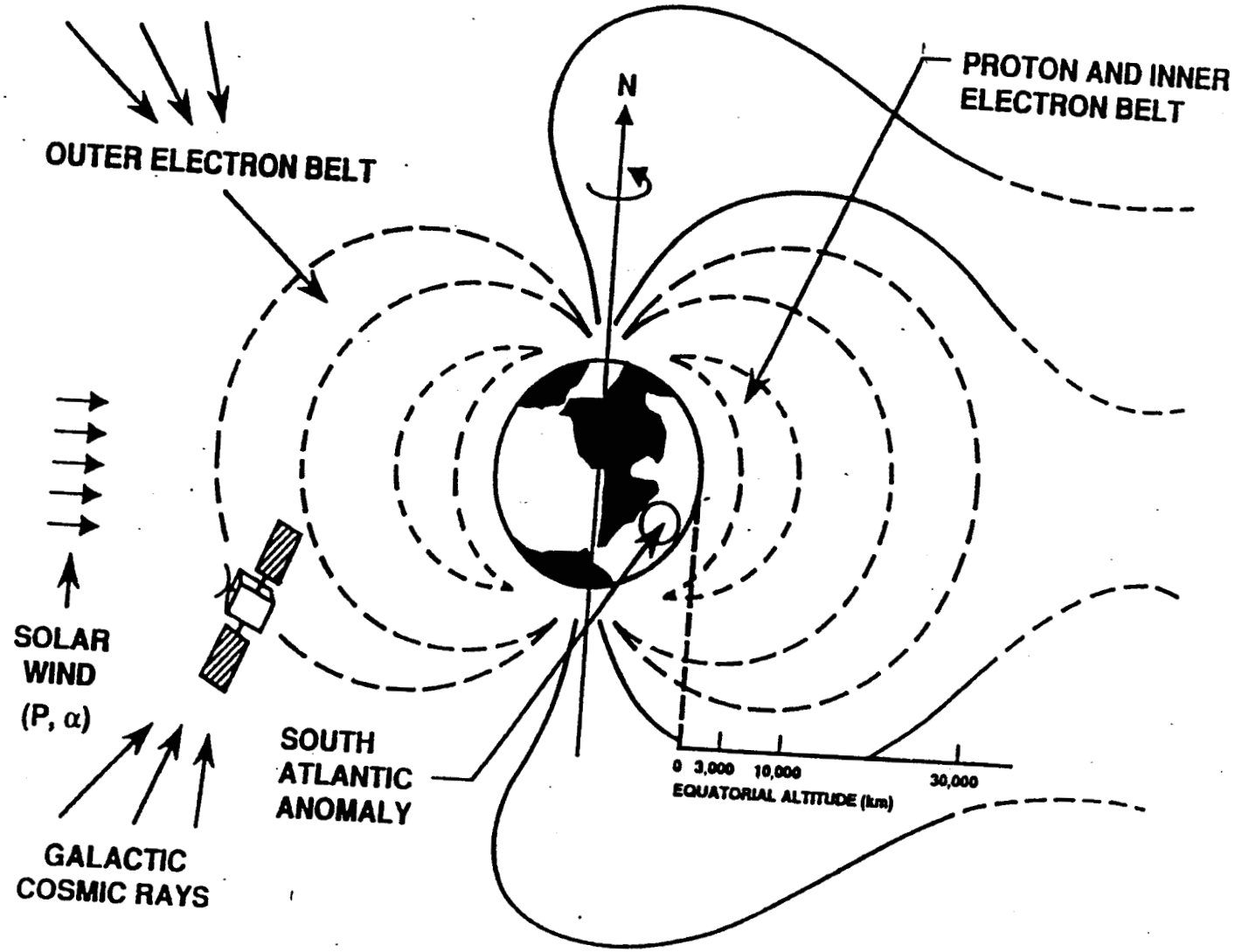


Figure 9.1. Magnetosphere Geometry

Earth's Van Allen Radiation Belts



Major Space Losses (1994-1998)

1994			
SATELLITE	CAUSE	LOSS	CLAIMS (M US$)
Anik E2	Electrical Discharge	Lifetime Loss	4.5
Eutelsat 2-F5	Ariane 4 Launch Failure	Total Loss	190.0
Türksat 1A	Ariane 4 Launch Failure	Total Loss	168.1
ETS-6	Apogee Motor Failure	Partial Loss	-
Telstar 402	Post Separation Failure	Total Loss	187.2
PAS-3	Ariane 4 Launch Failure	Total Loss	214.0
		Total	763.8

1995			
SATELLITE	CAUSE	LOSS	CLAIMS (M US$)
Apstar 2	CZ-2E Launch Failure	Total Loss	160.0
AMSC-1	East Beam Failure	Performance Loss	66.0
Koreasat 1	Delta 2 Low Performance	Lifetime Loss	64.4
GemStar	Athena 1 Launch Failure	Total Loss	11.6
Asiasat 2	Power Loss on Ku-band Transponders	Performance Loss	36.0
Meteor 1	Conestoga 1620 Launch Failure	Total Loss	5.3
		Total	343.3

1996			
SATELLITE	CAUSE	LOSS	CLAIMS (M US$)
Palapa C1	n.a.	Partial Loss	31.2
Intelsat 708	CZ-3B Launch Failure	Total Loss	219.3
MSat 1	Mountain Beam Failure	Partial Loss	109.0
Anik E1	Power Subsystem Failure	Total Loss	142.5
Cluster	Ariane 5 Launch Failure	Total Loss	-
Sirius 2	Soyuz Launch Failure	Total Loss	7.5
Chinasat 7	CZ-3 Launch Failure	Total Loss	128.0
HETESAC-8	Pegasus XL Separation Failure	Total Loss	tbd
Hot Bird 2	Apogee Transfer Anomaly	Lifetime Loss	19.9
Spot 3	Attitude Control Failure	Total Loss	13.0
		Total	665.4

1997			
SATELLITE	CAUSE	LOSS	CLAIMS (M US$)
Telstar 401	Electrical Discharge	Total Loss	132.0
Navstar	Delta 2 Launch Failure	Total Loss	35.1
B-Sat 1A	One Transponder Failure	Partial Loss	7.3
Adeos 1	Attitude Control Failure	Total Loss	-
Lewis	Loss of Attitude Control	Total Loss	-
Insat 2D	Power Subsystem Failure	Total Loss	62.1
JCSat 1	Propellant Leak	Lifetime Loss	25.5
Temipo 2	Electrical Discharge in Solar Arrays	Performance Loss	21.4
PAS-6	Electrical Discharge in Solar Arrays	Performance Loss	20.0
Asiasat 3	Proton K Launch Failure	Total Loss	215.0
EarlyBird 1	n.a.	Total Loss	29.0
		Total	547.4

1998			
SATELLITE	CAUSE	LOSS	CLAIMS (M US$)
Cometa	H-2 Launch Failure	Partial Loss	-
Kupon 1	n.a.	Total Loss	70.0
Calcrawarta 1	Battery Charging Anomaly	Performance Loss	n.a.
T1	n.a.	Temporary Loss	15.0 (a)
Iridium 24 & 71	In-Orbit Failures	Total Losses	59.0
Iridium 20 & 44	In-Orbit Failures	Total Losses	59.0
Echostar 4	Solar Array Failed to Deploy	Performance Loss	219.3
Eutelsat W1	Destroyed During Ground Tests	Cargo Loss	est. 50.0
Galaxy 4	Control Processor Failure	Total Loss	est. 180.0
Mercury 3	Titan 4A Launch Failure	Total Loss	70.0
Galaxy 10	Delta 3 Launch Failure	Total Loss	250.0
Globalstar	Zenit 2 Launch Failure	Total Loss	199.1
Echostar 3	TWTA Failures	Partial Loss?	tbd
JERS-1	Solar Array Anomaly	Total Loss	tbd
		Total	1,190.3

ESD Effects on Spacecraft Electronics

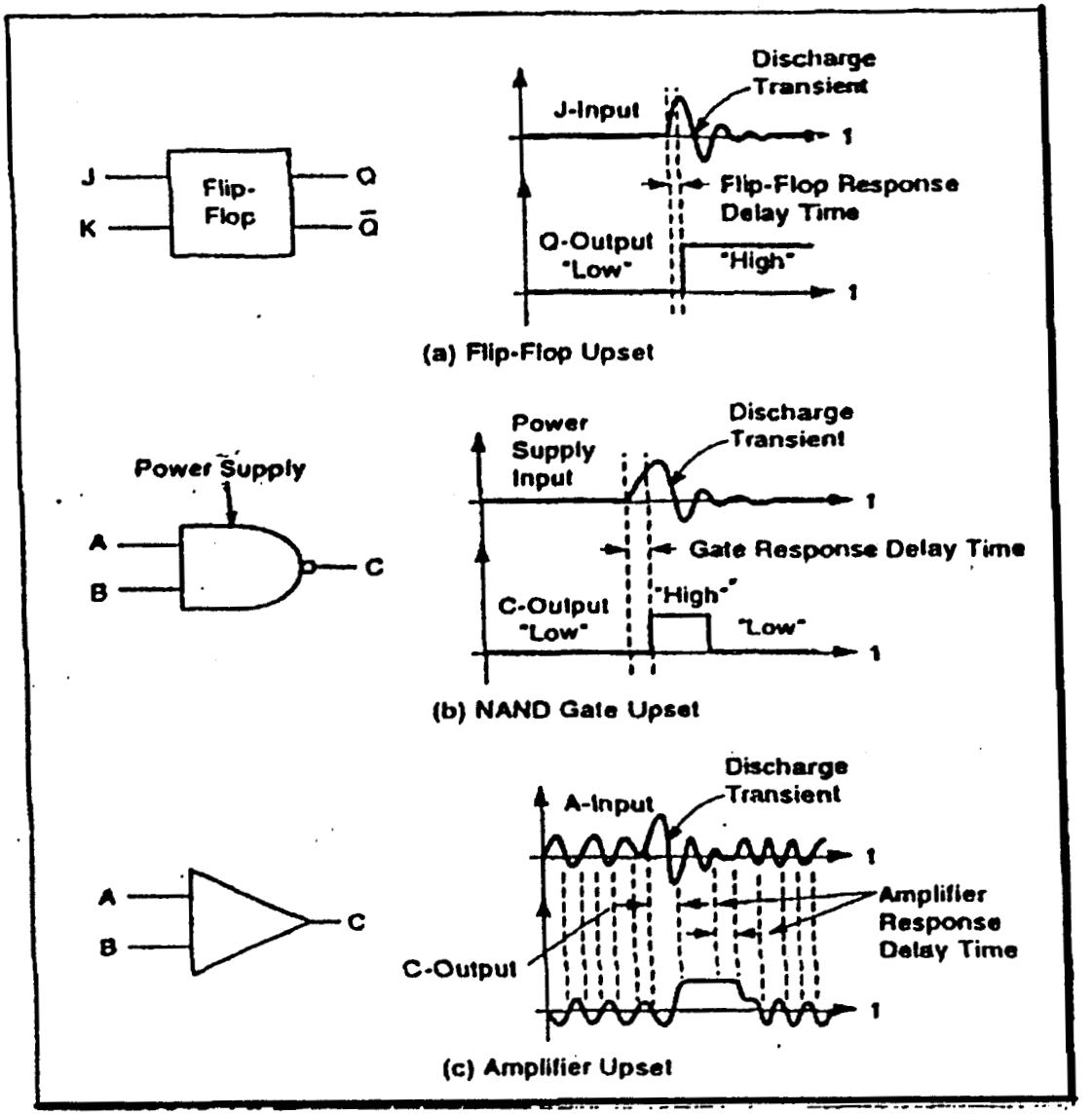


Figure 9.27. Examples of upset from discharges transients pulses.

The upset thresholds for representative logic families are given in Table 9.9. The upset level (e.g noise margin) for commonly used logic families vary from a few hundred milli-electron-volts to a few volts. Typical upset energy level threshold range from 1 to 50 nanojoules.

Logic Family	Power Supply (V)	Typical Gate Quiescent Power Dissipation (mW)	Typical Propagation Delay (nS)	Typical Signal Line DC Noise Immunity (V)				Typical Signal Line Impedance (ohms)		Logic Voltage Swing (V)	Typical Energy Noise Immunity on Signal Line (Joules x10^3)	
				Low		High						
				Min	Typ	Min	Typ	Low	High		Low	High
DTL	5	5	30	0.7	1.2	0.7	3.8	50	1.7K	4.5	3	15
TTL	5	15	10	0.4	1.2	0.4	2.2	30	140	3.5	4	25
HTL	15	30	85	5.0	7.5	4.0	7.0	140	16K	1.3	48	-
SCL	5.2	25	2	NA	0.2	NA	0.17	7	7	0.8	NA	NA
CMOS	5	0.000025	45	1.5	2.2	1.5	3.4	600	12K	5.0	3	15
CMOS	10	0.00010	16	3.0	4.2	3.0	6.0	300	600	10.0	10	5
CMOS	15	0.00023	12	4.4	6.5	4.5	9.0	250	450	15	22	13

Table 9.9. Typical Upset Threshold and Characteristics of Some Logic families

9.12 Component Damage

Component damage is a permanent change in one or more electrical characteristics of a circuit component. Circuit components are vulnerable to thermal damage and electrical breakdown when stressed by dielectric discharge transients. The damage energy threshold for various circuit components for a 100 nS rectangular transient pulse is shown in Figure 9.28. The damage threshold level ranges from 10 nJ for microwave diodes to several hundred nanojoules for various logic families.

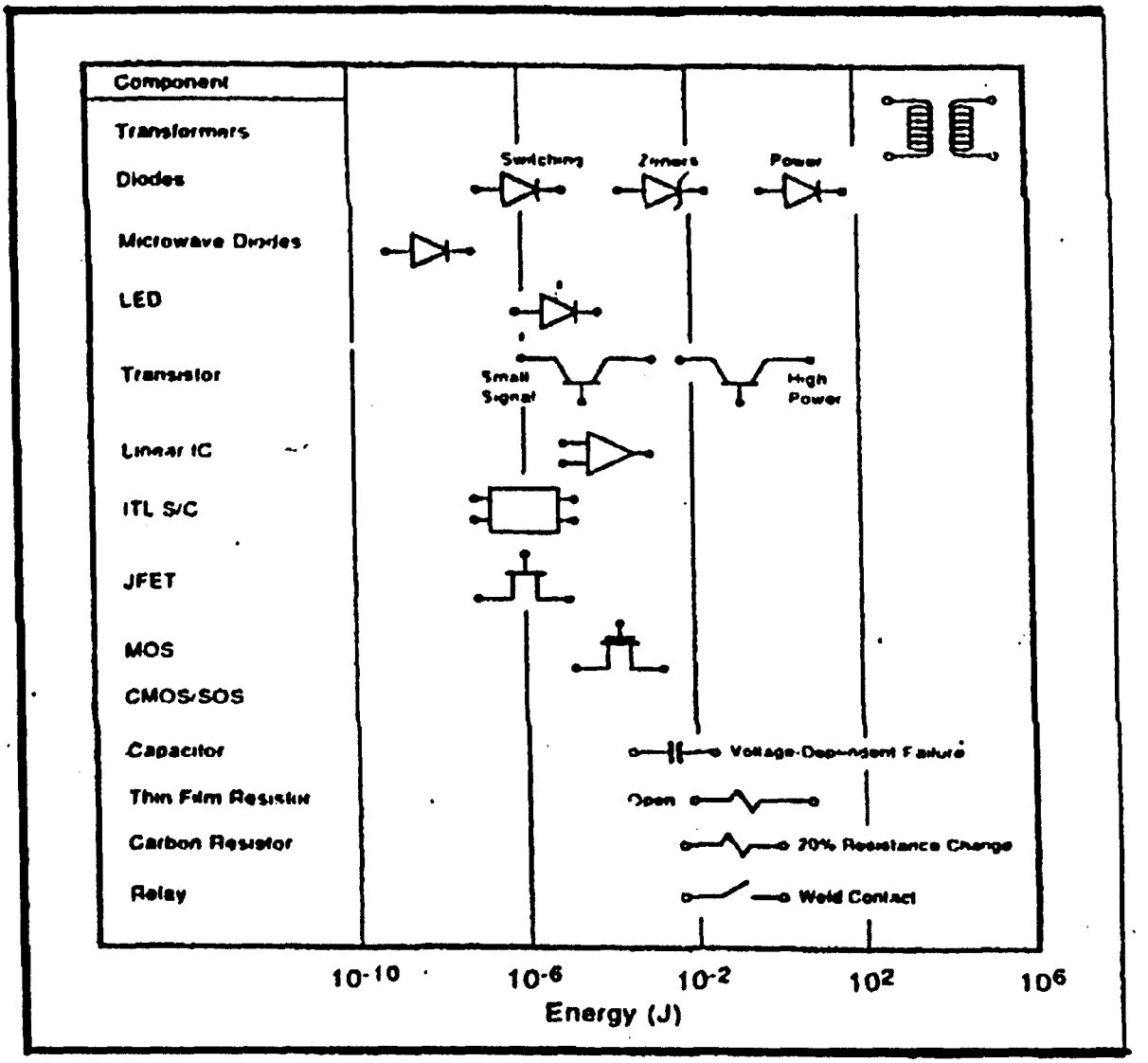


Figure 9.28. Permanent damage energy threshold of components for 100 nS pulse.

For semiconductors, the most common discharge transient damage mechanism is localized thermal runaway triggered by electro thermal over-stressed. This condition produces a resolidified melt channel across the junction once the transient is removed where the melt channel appears electrically as a low resistance shunt across the junction. Junction damage is most likely to occur when the discharge transient reverse biases the junction and drives it into second breakdown. Forward stressed junctions also fail but typically have damage thresholds that are three to ten times higher than reverse stressed junctions. For integrated circuits, metallization burnout and gate oxide breakdown (for MOS devices) are also prominent failure mechanisms.

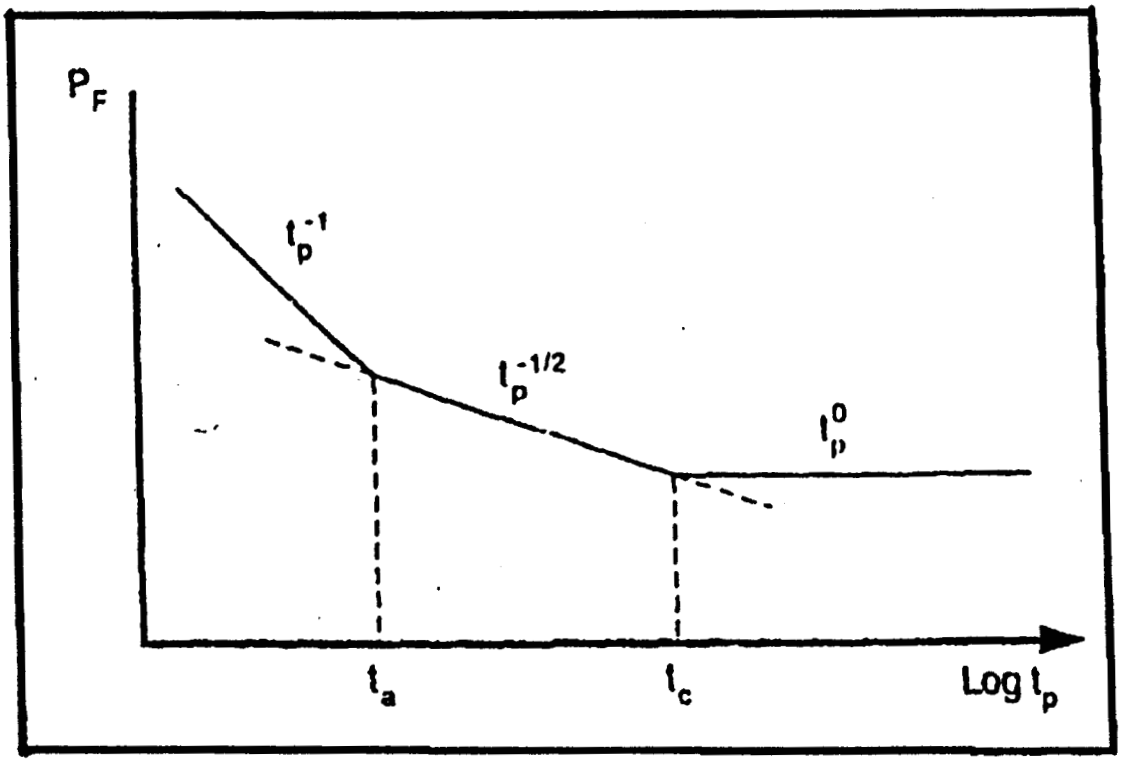


Figure 9.29. Pulse power failure depedence on pulse width for discrete semiconductors

Device	Type	K* (W $s^{1/2}$)	BV^{EBO} (V)	BV_{CBO} (V)	V_{BD}(V)
1N750A	Zener	2.84			4.7
1N756	Zener	20.4			8.2
1N914	Diode	0.096			75
1N3600	Diode	0.18			75
1N4148	Diode	0.011			75
1N4003	Diode	2.2			200
2N918	Transistor	0.0086	3	30	
2N2222	Transistor	0.11	5	60	
2N2857	Transistor	0.0085	2.5	30	
2N2907A	Transistor	0.1	5	60	
2N3019	Transistor	0.44	7	140	
2N3440	Transistor	1.1	7	300	

*$k_1 = k$, $k_2 = 1/2$

Table 9.10. Damage Constants and Junction Breakdown Voltages for Some Typical Discrete Semiconductors.

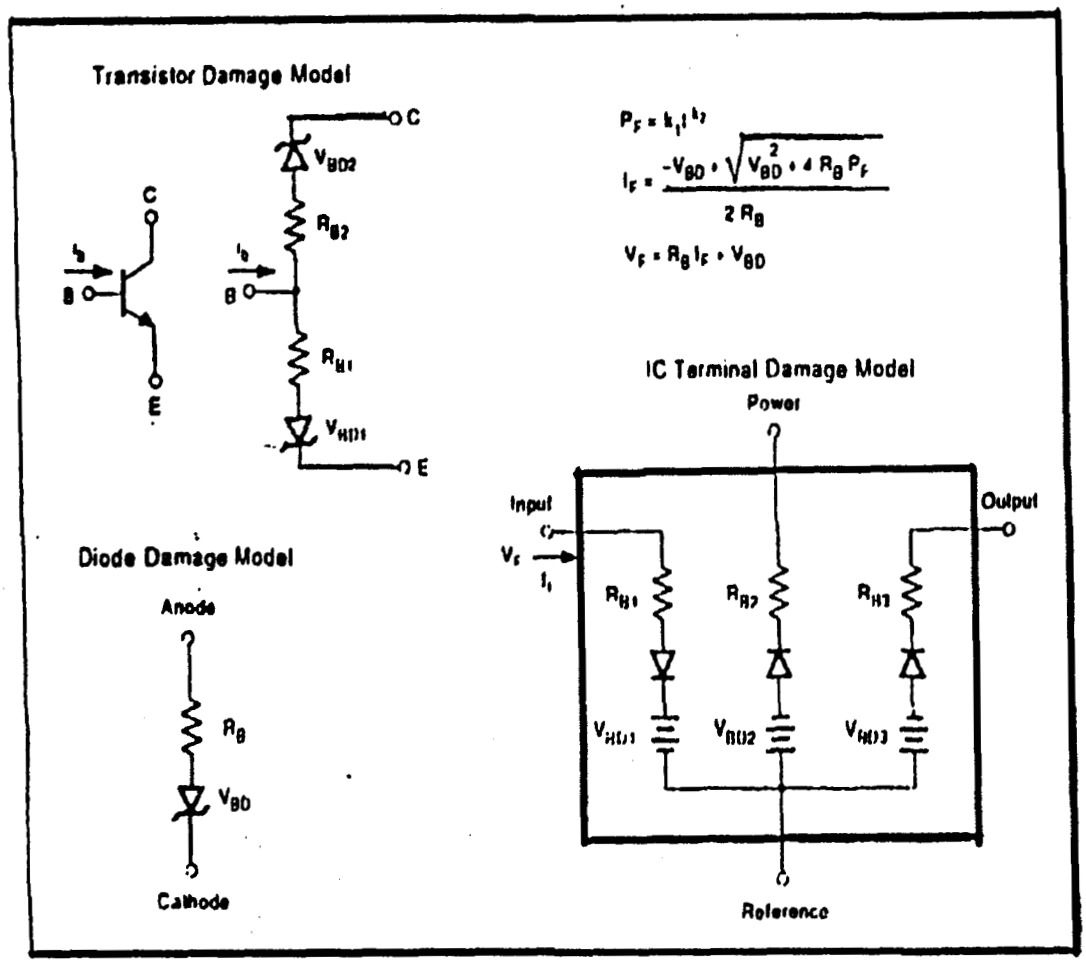


Figure 9.30. Transient pulse failure models for transistors, diodes, and integrated circuits

Device Category	Reverse Bias (ohms)	Forward Bias (ohms)
Zener diodes	1.0	0.1
Signal diodes	25.0	0.25
Rectifier diodes	150.0	0.05
Low frequency transistor (e-b)	10.0	1.0
High power transistor (e-b)	2.0	0.2

Table 9.11. Typical Junction Bulk Resistance for Discrete Semiconductors

For integrated circuits, k_1 and k_2 are determined experimentally when possible. For the case where test data is not available, typical values of these coefficients for different types of integrated circuits have been determined by tests and are given in Table 9.12. Tight integrated circuit manufacturing tolerances and standard circuit designs have allowed integrated circuits to be

grouped by their technology into genetic failure classes and their terminals categorized into one of the following types: input terminal, output terminal, and power terminal. The IC terminal failure model consists of a resistor representing the terminal's bulk resistance and voltage source representing the terminal's reverse breakdown voltage.

	Category		K_1	K_2	V_{BD} (V)	R_B (ohms)	Lower 95% K_1	Upper 95 K_2
	Family	Terminal						
	TTL	Input	0.00216	0.689	7	16	0.00052	0.00896
		Output	0.00359	0.722	1.3	2.4	0.00098	0.013
	RTL	Input	0.554	0.384	6	40	0.12	2.6
		Output	0.0594	0.508	5	18.9	0.0096	0.39
		Power	0.0875	0.555	5	20.8	0.026	0.70
	DTL	Input	0.0137	0.580	7	25.2	0.0046	0.041
		Output	0.0040	0.706	1	15.8	0.012	0.0136
		Power	0.0393	0.576	1	30.6	0.009	0.17
	ECL	Input	0.152	0.441	20	15.7	0.045	0.51
		Output	0.0348	0.558	0.7	7.8	0.0031	0.397
		Power	0.456	0.493	0.7	8.9	0.22	0.935
	MOS	Input	0.0546	0.483	30	9.2	0.0063	0.47
		Output	0.0014	0.819	0.6	11.6	0.00042	0.0046
		Power	0.105	0.543	3	10.4	0.038	0.29
	Linear	Input	0.0743	0.509	7	13.2	0.0054	1.01
		Output	0.0139	0.714	7	5.5	0.0045	0.043

Table 9.12. Damage Constants and Failure Parameters for Various Logic families.

From the failure models for discrete semiconductors and integrated circuits, we find the failure voltage, V_F, and failure current I_F, at the device terminals are expressed as

$$V_F = V_B + I_F R_B$$
$$I_F = \left(V_B - \sqrt{V_B^2 - 4R_B P_p}\right) / 2R_B \qquad (9.9)$$

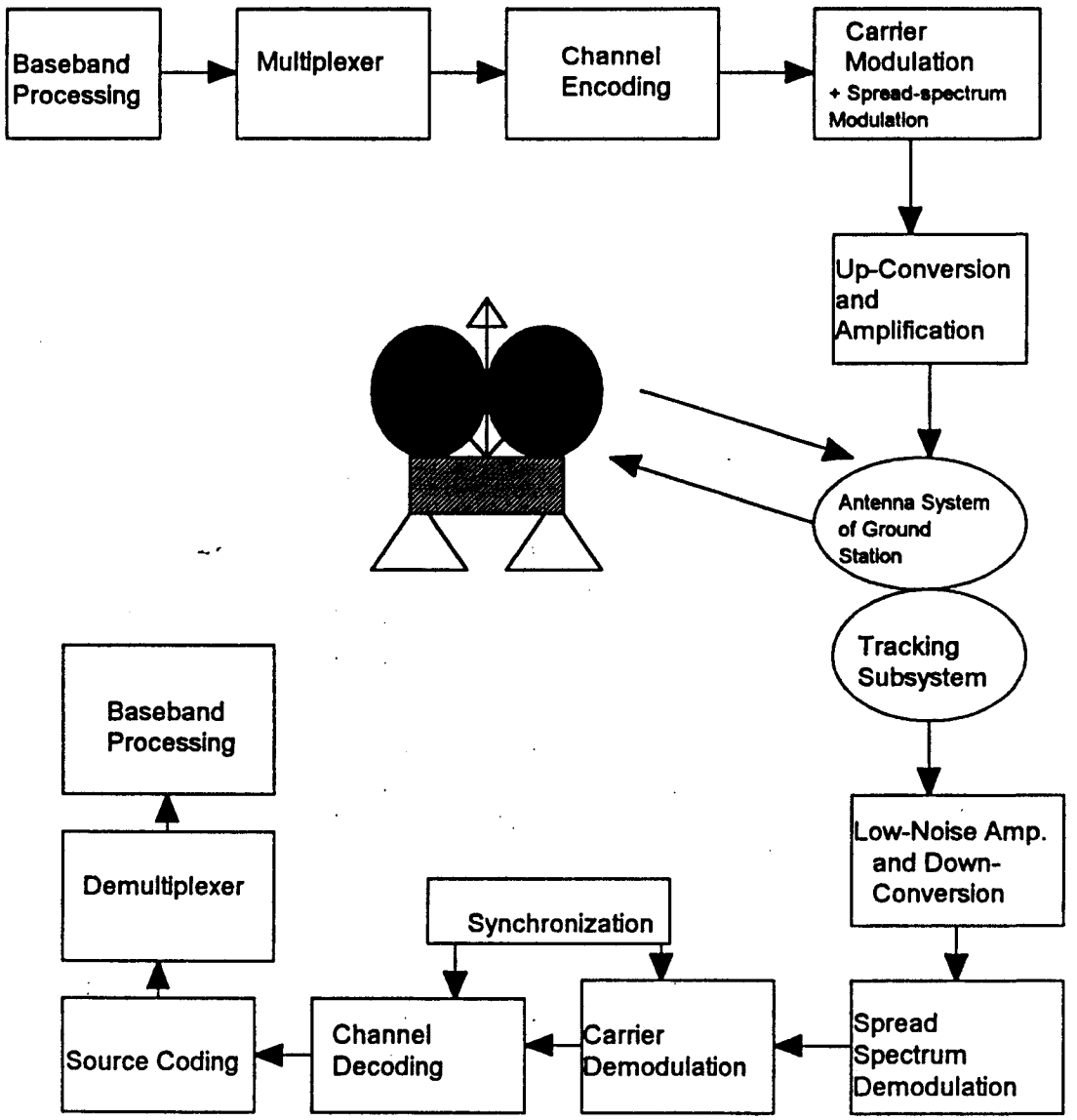
where V_B is the terminal's breakdown voltage, R_B is the terminal's bulk resistance and P_p is the terminal's failure power given previously. The conditions for failure to occur when a circuit is stressed by a discharge transients is as follows:

1) the discharge transient current produced at the terminals of the transistor, diode, or integrated circuit must be equal to or exceed I_F/D where I_F is obtained from equation 9.9 above. D is a derating factor to account for statistical variations in device failure thresholds. D is 3 for P_p values

ESD Effects on Radio Systems

Electromagnetic "issues" in Satellites

1) INTERFERENCE
2) REFLECTOR ANTENNA SIZES AND POINTING
3) MAGNETIC EFFECTS
4) PROPER ANTENNA DESIGN
   (phase arrays, horns, helices, spiral, parabolic multibeam)
5) RF POWER TRANSMISSION (s/n)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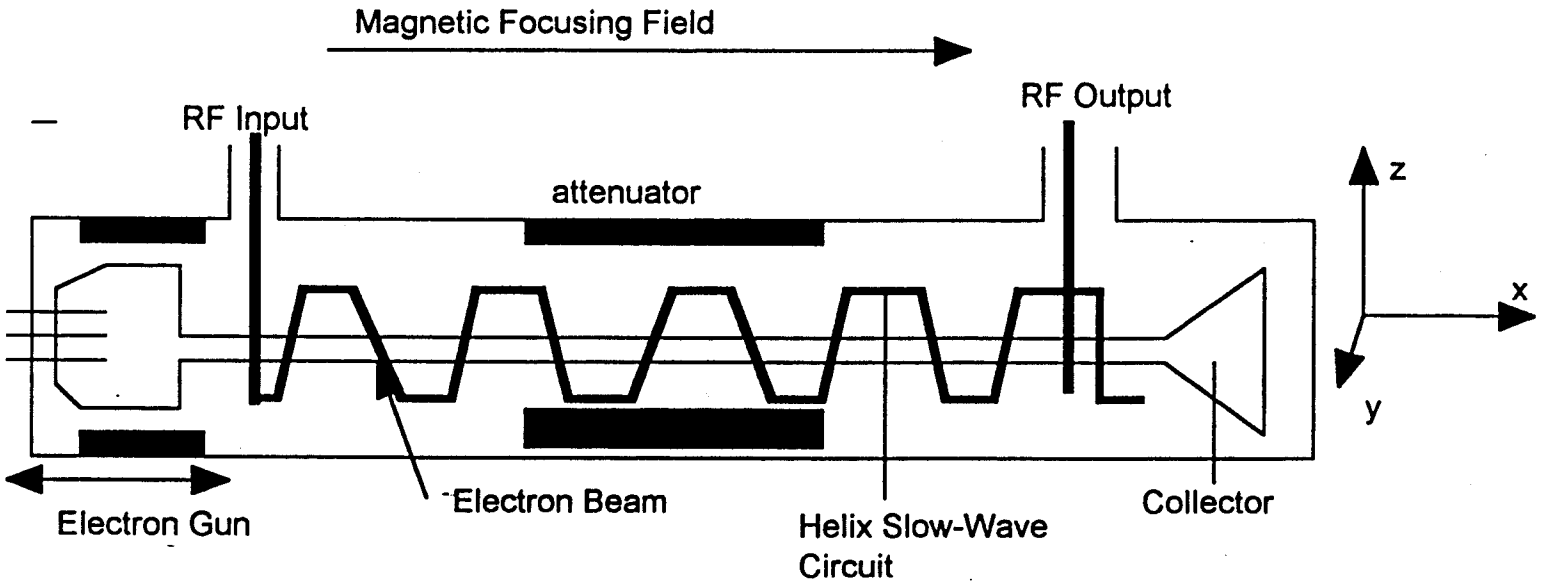
Multiplexer
Channel Encoding
Carrier Modulation
+ Spread-spectrum Modulation
Up-Conversion and Amplification
Antenna System of Ground Station
Tracking Subsystem
Low-Noise Amp. and Down-Conversion
Spread Spectrum Demodulation
Carrier Demodulation
Synchronization
Channel Decoding
Source Coding
Demultiplexer
Baseband Processing


Magnetic Focusing Field
RF Input
RF Output
attenuator
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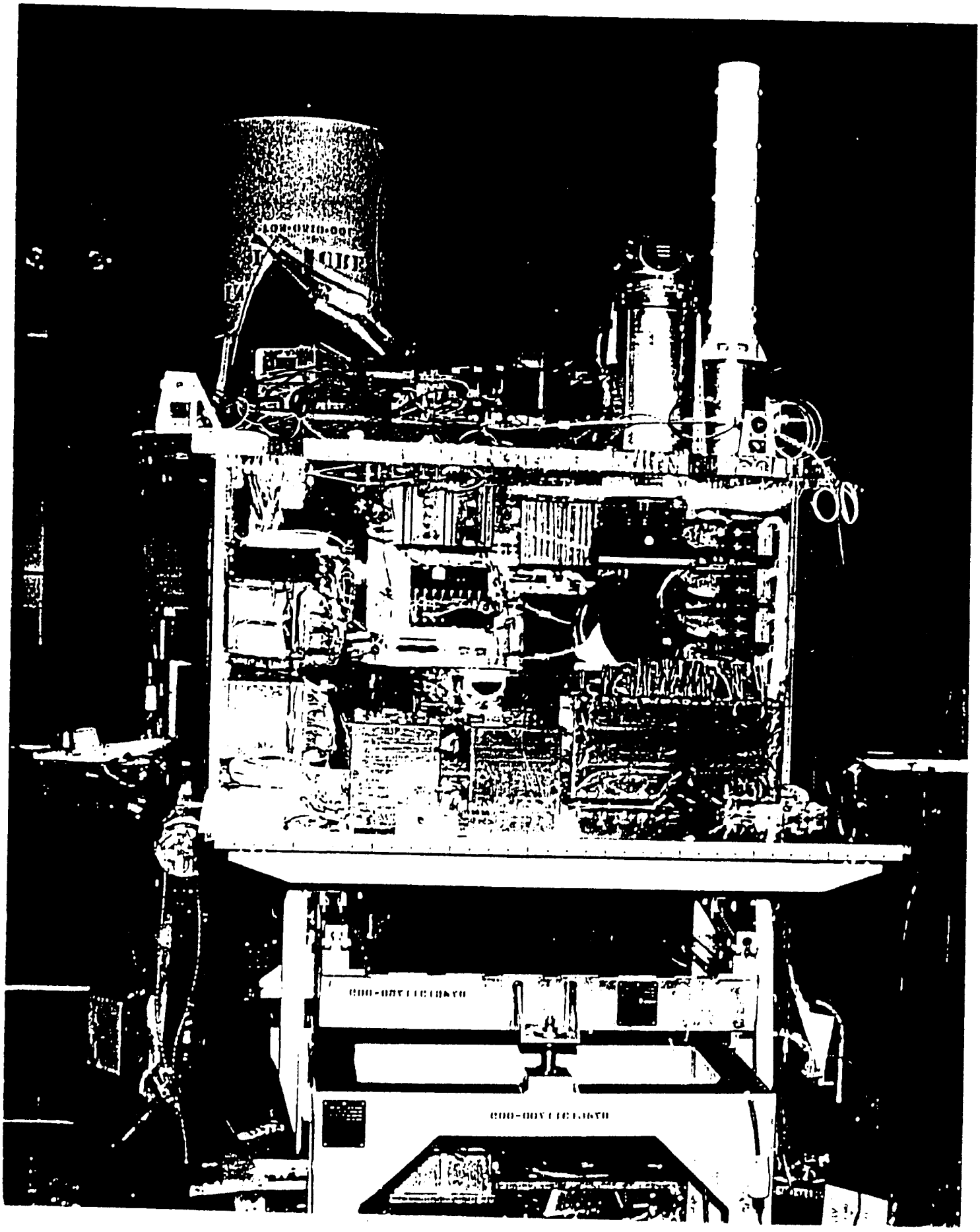
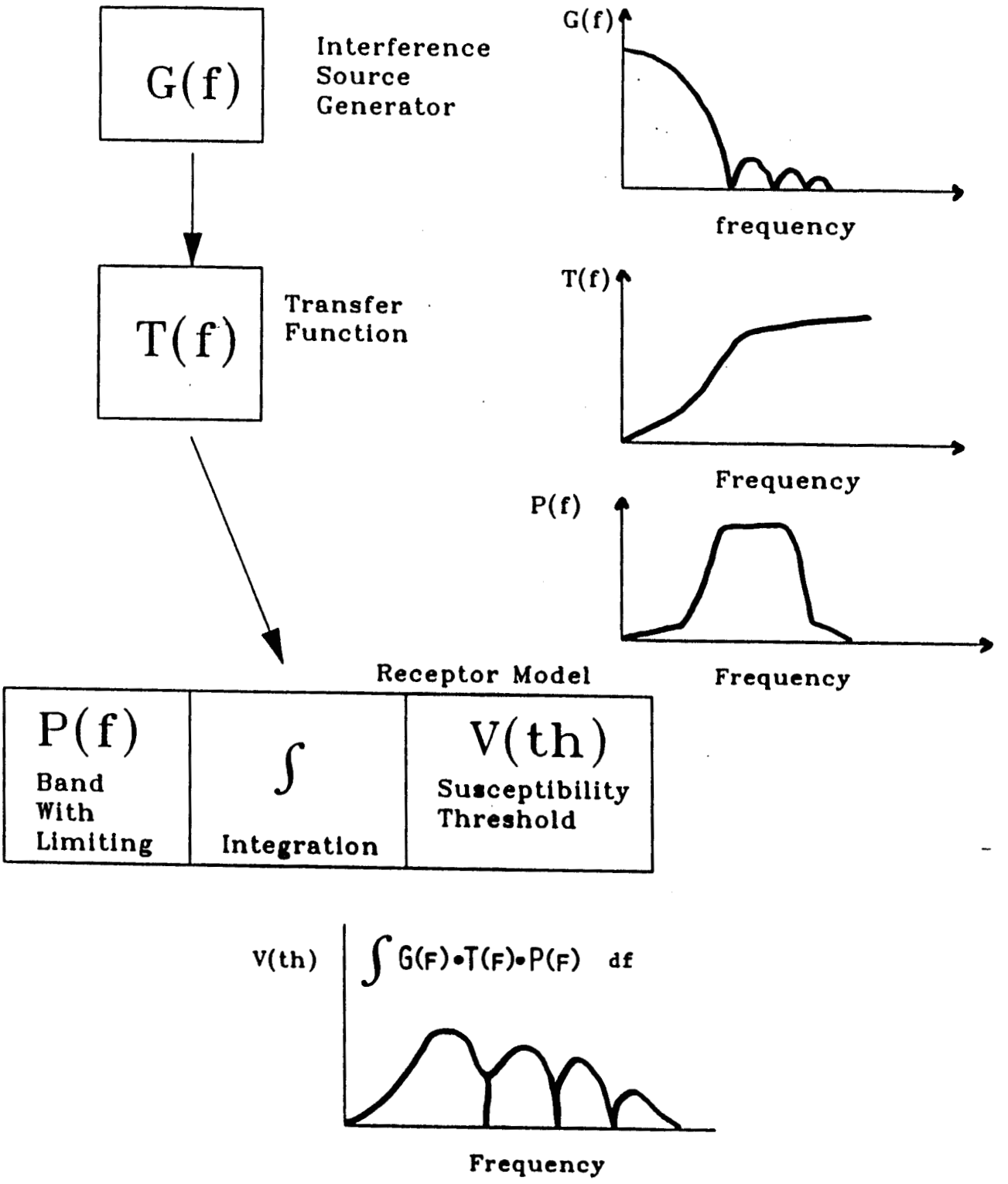
Electron Gun
Electron Beam
Helix Slow-Wave
Circuit
Collector



LEO ORBITS

Modeling and Analysis of ESD Events


G(f)
Interference
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G(f)
frequency
T(f)
Transfer
Function
T(f)
Frequency
P(f)
Frequency
Receptor Model
P(f)
Band
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Limiting
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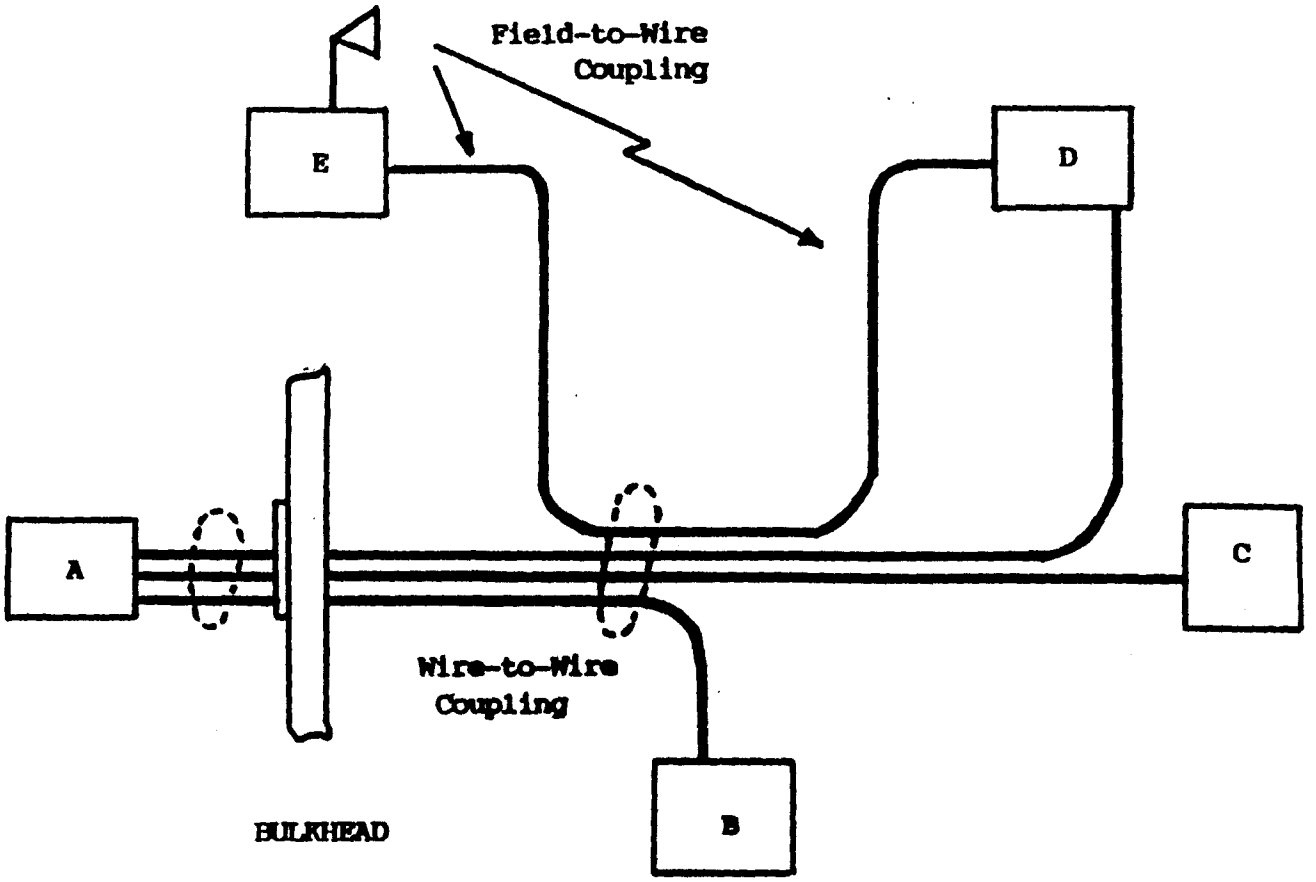
V(th)
Susceptibility
Threshold
V(th)
∫ G(F)•T(F)•P(F) df
Frequency


Field-to-Wire
Coupling
E
D
A
C
Wire-to-Wire
Coupling
BULKHEAD
B

RFI PROBLEMS IN TRANSMITTERS	BRIEF DESCRIPTION OF RFI PROBLEM	METHODS OF SUPPRESSION
Sideband Splatter[1]	Deviations from the required response law in the transmitter modulator causing spectrum broadening. AM/FM, SSB, DSB systems.	- Filtering
Internal Harmonic Generation[2]	Deviations from the linearity of a transmitter final amplifier	-Balanced circuits -Filtering -Wave trap
Intermodulation and Cross modulation[3]	Mixing of two or more signals in a non linear element. Resulting multiplicative mixture of both signals	-Filtering
Oscillator Noise	Similar to sideband splatter except at a lower level	-Filtering -Design of very good oscillators

In Table 1a the following applies:

(1) Output of nonlinear element plus narrowband filter centered at carrier ω_c. Input function is X_1.

$$\sum_{n=1}^{N} \sum_{k=1}^{n} a_n \binom{n}{k} X_1^{n-k} \frac{k!}{\left(\frac{k-1}{2}\right)! \left(\frac{k+1}{2}\right)!} Cos(\omega_c + \phi_c)$$

(2) output of nonlinear device is

$$y = a_o + a_1 x + a_2 x^2 + \ldots + a_k x^k$$

$$where \quad x = x_1(t) + Cos\ w_c\ t$$

(3) Let Signal 1

$$X_1(t) = m_1(t)\ Cos\ (\omega_1 t + \phi_1(t))$$

Let Signal 2

$$X_2(t) = m_2(t)\ Cos\ (\omega_2 t + \phi_2(t))$$

$X(t) = X_1(t) + X_2(t)$ go through a nonlinear device to obtain the result

$$y(t) = a_o + a_1 x + a_2 x^2 + a_3 x^3$$

For intermodulation:

$$y(t) = m_1^2(t)\ Cos[(2\omega_1 - \omega_2) + 2\phi_1(t) - \phi_2(t)]$$

For crossmodulation:

$$y(t) = m_1^2(t)\ m_2(t)[Cos\ \omega_2 t + \phi_2(t)]$$

Table 1a. FRI PROBLEMS IN TRANSMITTERS.

RFI PROBLEM IN RECEIVERS	BRIEF DESCRIPTION OF PROBLEM	METHOD OF SUPPRESSION
Broadband Noise	Noise from natural sources (thermal, shot, solar, atmospheric) or man-made (discharges, switching of electronic devices, antenna behavior)	-Limiting & blanketing before broadband noise is filtered in the IF amplifier
Co-Channel Interference	Signal from communication sources are assigned a frequency near the center frequency of receiver	-Good care in frequency assignment
IF Channel Interference	Penetration of unwanted signals centered at one of the IF channels of the receiver	-Selective of the input RF circuit and/or stray paths must be controlled
Spurious Response[4]	Nonlinearities in early stage gives rise to harmonics of incoming signals; nonlinearities in the mixer and frequency multiplication in local oscillator	-Filtering prior to mixer
Intermodulation & Crossmodulation	Intermodulation: when two or more unwanted signals are present at the input. crossmodulation:transfer of information from an undesired carrier onto the desired one	-Filtering
Desensitization	Reduction of receiver gain when a large unwanted signal enters the receiver	-Filtering prior to receiver

In Table 1b the following applies:

(4) Mixing operation:

if oscillator is $y_1 = A \cos \omega_1 t$

and signal is $y_2 = x_s(t) \cos (\omega_s t + \phi_s)$

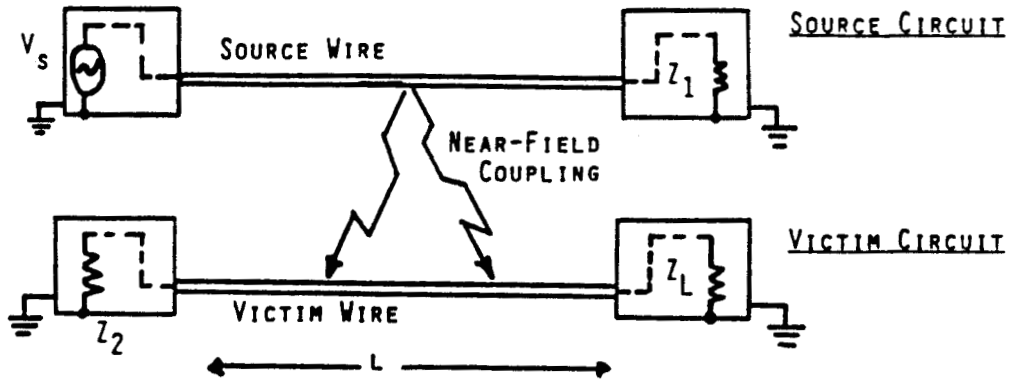
For non linearity

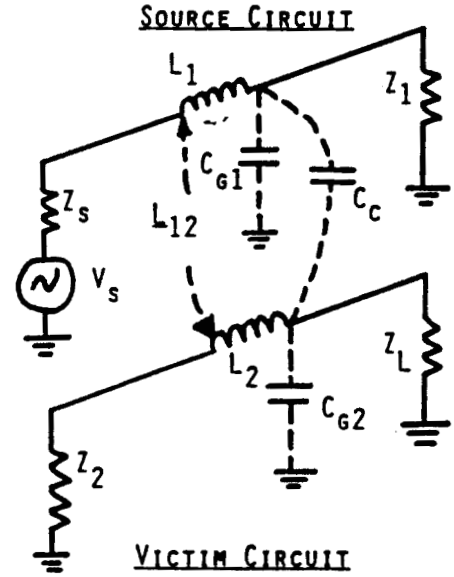
$$y = \sum_{n=0}^{N} b_n y^n$$

and the result of $y = y_1 + y_2$ *is*

$$\sum_{n=0}^{N} b_n \sum_{k=0}^{n} \binom{n}{k} x_s^k(t) \cos^k (\omega_s t + \phi_s) A^{(n-k)} \cos^{(n-k)} \omega_1 t$$

Table 1b. FRI PROBLEMS IN RECEIVERS.





L=LENGTH OF WIRES
L_1 = WIRE INDUCTANCE OF SOURCE CIRCUIT
Z_S = IMPEDANCE OF SOURCE CIRCUIT
C_{G1} = CAPACITANCE TO GROUND IN SOURCE CIRCUIT
V_S = VOLTAGE OF SOURCE CIRCUIT
Z_1 = LOAD IMPEDANCE OF SOURCE CIRCUIT
C_C = COUPLING CAPACITANCE
Z_2 = SOUCE IMPEDANCE OF VICTIM CIRCUIT
Z_L = LOAD IMPEDANCE OF VICTIM CIRCUIT
C_{G2} = CAPACITANCE TO GROUND IN VICTIM CIRCUIT
L_{12} = MUTUAL INDUCTANCE

$$V(Z_L) = \frac{j2\pi f l \frac{Sin(\beta L)}{\beta L} Z_L[C_c Z_1 Z_2 - L_{12}] V_s}{[---]}$$

$$V(Z_2) = j2\pi f l \frac{Sin(\beta L)}{\beta L [---]} Z_2\Big[[Cos(\beta L)[Z_L Z_1 C_c + L_{12}]] + j2\pi f l \frac{Sin(\beta L)}{\beta L}[Z_L C_c L_1 + Z_1 L_{12}(C_{g1}$$

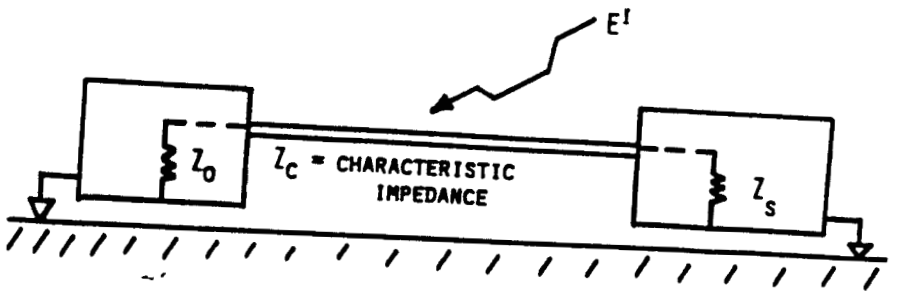
where

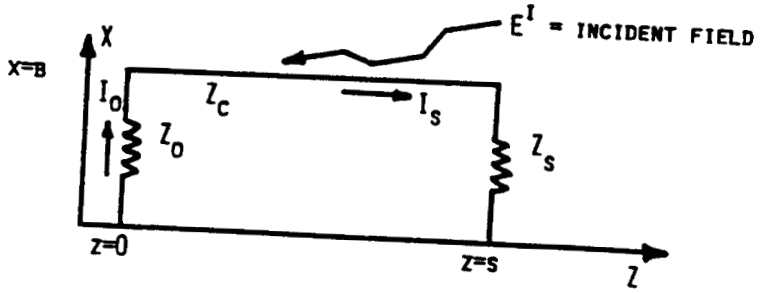
$$[---] = (Z_s + Z_1)(Z_2 + Z_L) Cos^2(\beta L) -$$

$$j4\pi^2 f^2 l^2 \frac{Sin^2(\beta L)}{(\beta L)^2}[[Z_1 Z_s (C_{g1} + C_c) + L_1][Z_2 Z_L (C_{g2} + C_c) + L_2] - [L_{12} - C_c Z_s Z_1][L_{12} - C_c C_1 Z_2]] +$$

$$j2\pi f \frac{Sin(\beta L)}{\beta L} Cos(\beta L)[(Z_2 + Z_L)[Z_1 Z_s (C_{g1} + C_c) + L_1] + (Z_s + Z_1)[Z_2 Z_L (C_{g2} + C_c) + L_2]]$$

Figure 1. CAPACITIVE & INDUCTIVE NEAR FIELD COUPLING





$$I_o = \frac{1}{[---]} \int_0^s P(z)\,[Z_c Cosh\gamma(z-s) - Z_s Sinh\gamma(z-s)]\,dz -$$

$$\frac{Z_c}{[---]} \int_0^b E_x^i(x, s)\,dx + \frac{Z_c Cosh\gamma s + Z_s Sinh\gamma s}{[---]} \int_0^b E_x^i(x, 0)\,dx$$

$$I_s = \frac{1}{[---]} \int_0^s P(z)\,[Z_c Cosh\gamma(z) - Z_o Sinh\gamma(z)]\,dz -$$

$$\frac{Z_c}{[---]} \int_0^b E_x^i(x, 0)\,dx + \frac{Z_c Cosh\gamma s + Z_o Sinh\gamma s}{[---]} \int_0^b E_x^i(x, s)\,dx$$

where

$$P(z) = \left[E_x^i(b, z) - E_x^i(0, z)\right]$$

$$[---] = [Z_c Z_o + Z_s Z_c] Cosh\gamma s + [Z_c^2 + Z_s Z_o] Sinh\gamma s$$

Figure 2. FIELD TO WIRE COUPLING

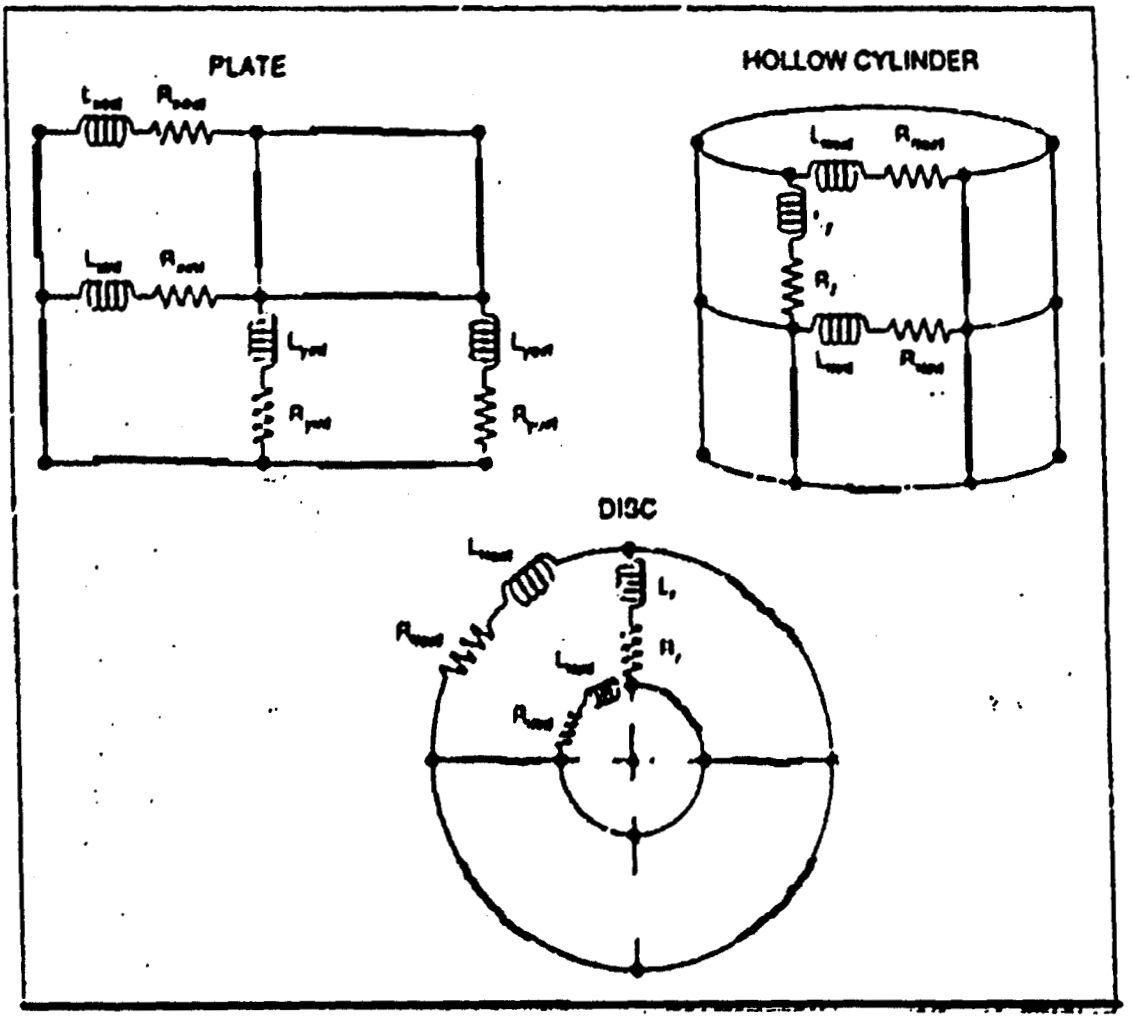


Figure 9.26. Equivalent circuits for plates, cylinder, and disc.

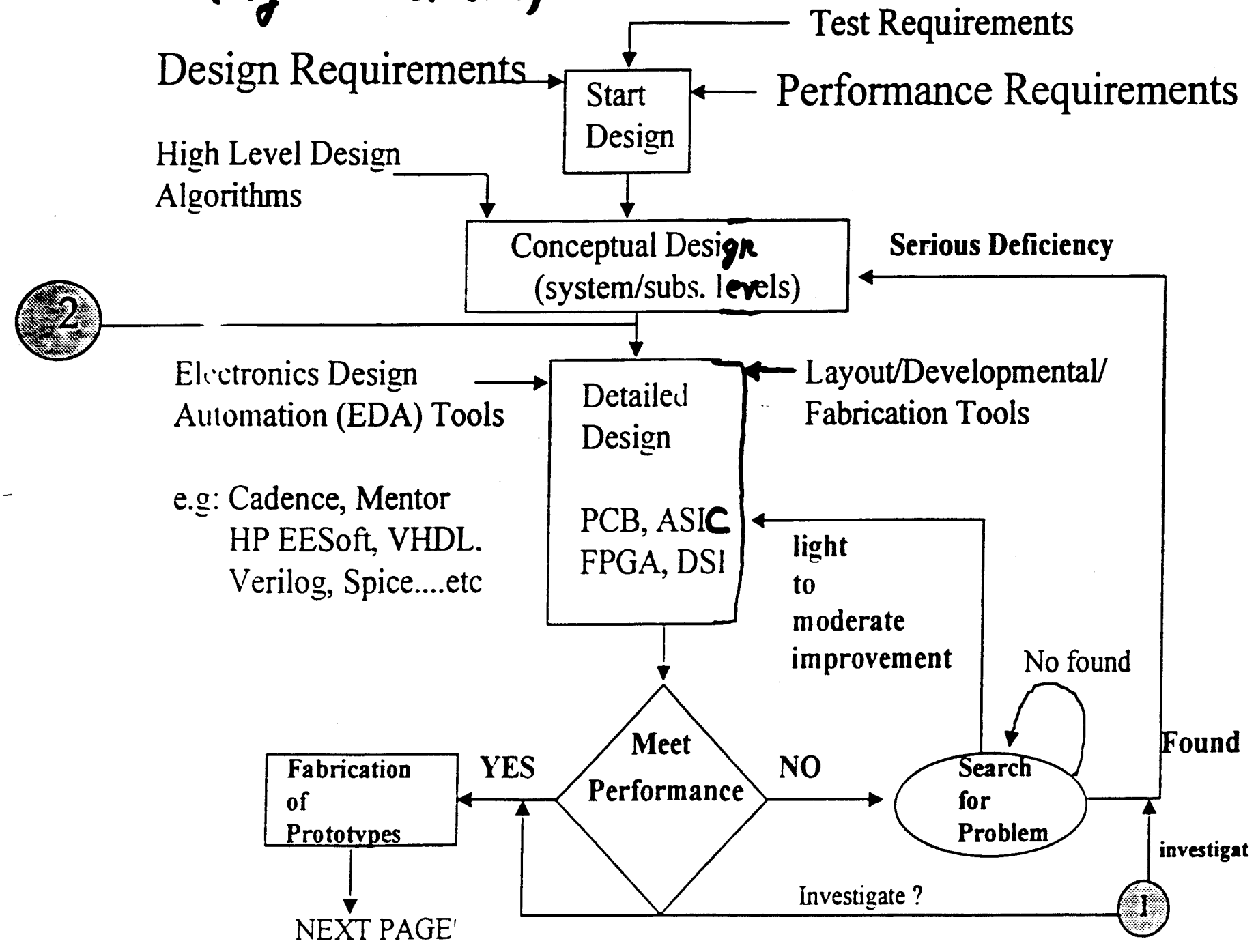
9.11 Circuit Upset.

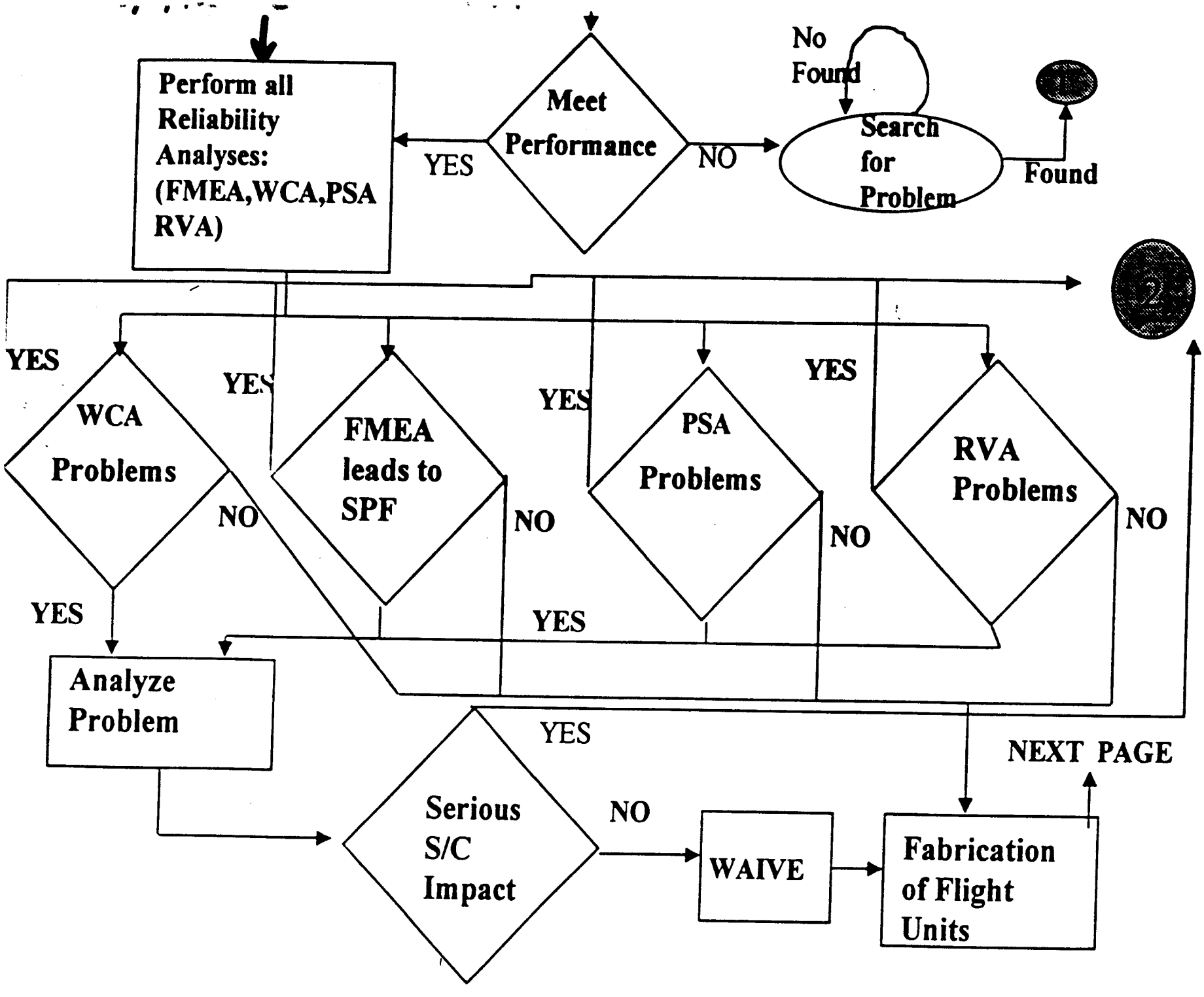
Circuit upset is a nonpermanent alteration of a circuit or component operational state that is self-correcting or reversible by automatic or manual means. Some examples of upset are provided in Figure 9.27. The conditions for upset to occur when a circuit is stressed by a discharge transient are as follows:

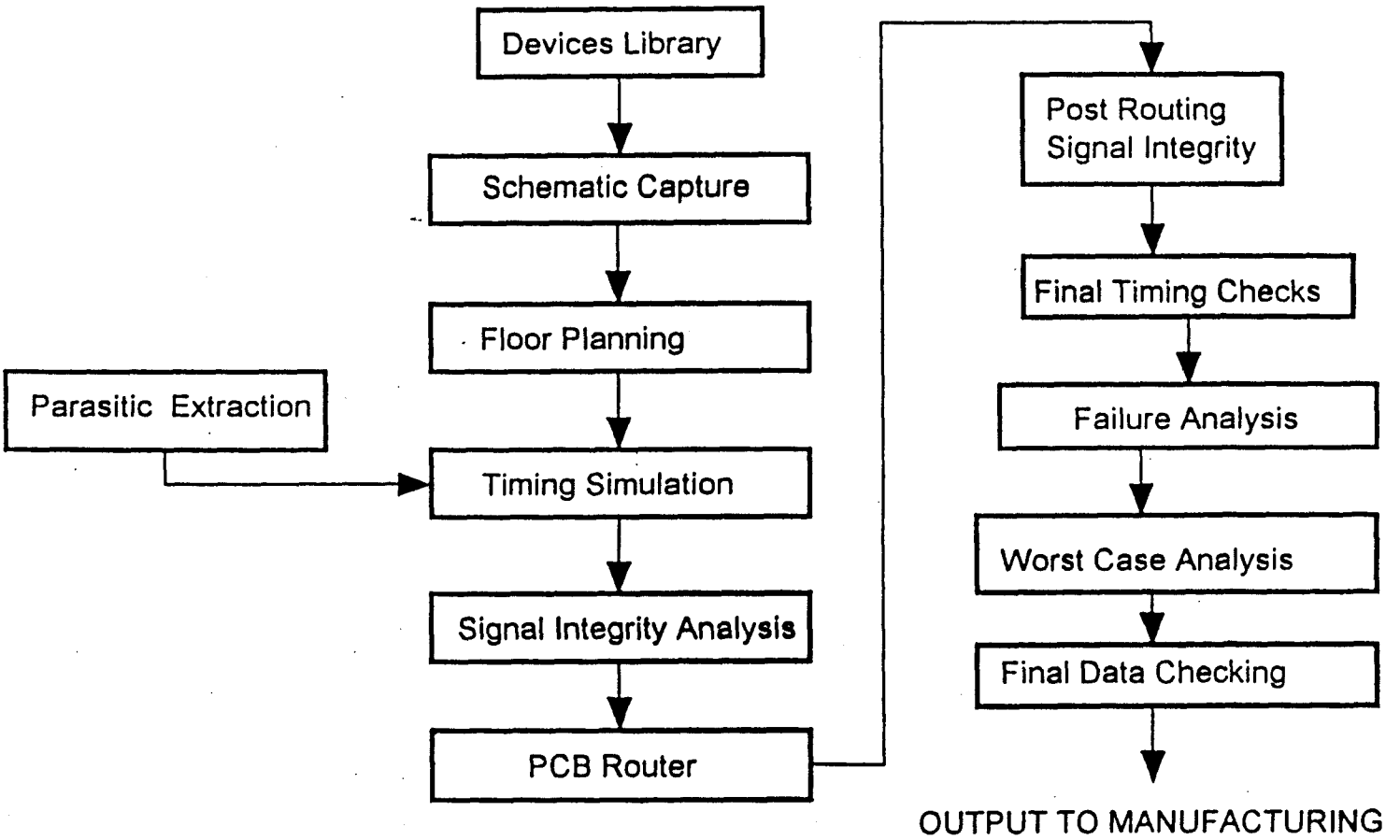
Conclusion

Present Approach to Designing/Building Spacecraft Electronics

(e.g Pathfinder)




Perform all Reliability Analyses: (FMEA,WCA,PSA RVA)
Meet Performance
YES
NO
No Found
Search for Problem
Found
1
2
YES
WCA Problems
NO
YES
FMEA leads to SPF
NO
YES
PSA Problems
NO
YES
RVA Problems
NO
YES
YES
Analyze Problem
YES
Serious S/C Impact
NO
WAIVE
Fabrication of Flight Units
NEXT PAGE



A RELIABLE PCB DESIGN PROCESS THAT ASSURES "RIGHT THE FIRST TIME" PERFORM